ERSA'12 CONFERENCE SCHEDULE

The 2012 International Conference on Engineering of Reconfigurable systems and Algorithms

Monte Carlo Resort, Las Vegas, Nevada, July 16 -19, 2012

There are number of other conferences and sessions (not listed as part of ERSA schedule) that are of potential interest to ERSA conference participants. Therefore, you are encouraged to check the schedules for other WORLDCOMP conferences. In particular, PDPTA, GCA, CDES, ESA, FECS, etc., discuss the topics that are within the scope of ERSA.

July 16

6:30am - 5:00pm: **REGISTRATION (Second Floor, Conference Lobby: 1-5)**

08:30 - 08:45am: **Congress Opening Remarks - July 16, Monday:**
Prof. Hamid R. Arabnia (Chair, Steering Committee & Coordinator)
University of Georgia, Georgia, USA
(LOCATION: Monte Carlo Pavilion)

08:50 - 09:45am: **Keynote Lecture 1 - July 16, Monday:**
Teaching Software Engineering for Software as a Service using Massive
Open Online Courses
Professor David A. Patterson
University of California at Berkeley, California, USA
Member, National Academy of Engineering
Member, National of Academy of Sciences
Fellow of IEEE, ACM, and AAAS
Shared (with John Hennessy) the IEEE John von Neumann Medal
(LOCATION: Monte Carlo Pavilion)

09:55 - 10:50am: **Keynote Lecture 2 - July 16, Monday:**
Crowdsourcing, Human Computation, and Collective Intelligence
Professor Haym Hirsh
Rutgers University, New Jersey, USA
Former Director (2006-2010) of Division of Information and Intelligent
Systems, National Science Foundation, USA + Visiting Scholar (2010-2011)
at MIT's Center for Collective Intelligence, USA.
Prof. Hirsh received
his PhD in 1989 from Stanford University.
(LOCATION: Monte Carlo Pavilion)

11:00 - 11:55am: **Keynote Lecture 3 - July 16, Monday:**
ECL and Distributed Machine Learning with the HPCC Systems Platform
Dr. Flavio Villanustre
Vice-President of Technology Architecture and Product,
HPCC Systems (Dr. Villanustre's previous profession was a neurosurgeon).
(LOCATION: Monte Carlo Pavilion)

12:00 - 01:00pm: **LUNCH (On Your Own)**

01:00 - 01:20pm: **ERSA'12 Opening remarks**
Dr. Toomas P. Plaks, ERSA Chair
(LOCATION: Gold Room)

01:20 - 02:20pm: **ERSA Keynote**
Towards OpenCL Compilation into High-Performance Hardware for FPGAs
Prof. Stephen Brown, University of Toronto & Altera, Canada
Moderator: Dr Pascal Benoit, Electrical Engineering department of University of Montpellier, France
(LOCATION: Gold Room)

SESSION A: **REGULAR SESSION**
APPLICATIONS
Chair: Prof. Franz Richter, FAU Erlangen-Nuremberg, Germany
July 16, 2012 (Monday): 01:40pm – 04:40pm
(LOCATION: Gold Room)

02:20 - 03:00pm: **Invited Talk**
Future Internet Infrastructure and its Hardware Support Technology for Smart Grid
Prof. Hiroaki Nishi
Department of System Design, Keio University, Japan

03:00 - 03:20pm: **BREAK**

03:20 - 04:20pm: **ERSA Industrial Keynote**
Software-Based Reconfigurable Computing Platform (AppSTARTM) for Multi-Mission Payloads in Spaceborne and Near-Space Vehicles
Dr. Edward R. Beadle and Dr. Tim Dyson
Harris Corporation, Government Communications Systems Division, USA

04:20 - 04:40pm: Implementation of a Hardware Architecture to Support High-speed Database Insertion on the Internet
Yusuke Nishida, Hiroaki Nishi
Department of Science and Technology, Keio University, Yokohama, Kanagawa, Japan

04:40 - 06:00pm: **PANEL DISCUSSION & SHORT STATEMENTS**
HIGH LEVEL DESIGN FOR FPGAS:
OPENCL, SPACE CODESIGN, CUDA ...
Chair: Prof. Stephen Brown, University of Toronto & Altera, Canada

06:00 - 09:00pm: **TUTORIALS + INVITED PRESENTATIONS**
(Please see the lists at the beginning of the WORLDCOMP'12 Conference Schedules)

09:10 - 11:30pm: **CONFERENCE RECEPTION DINNER / SOCIAL**

July 17

6:45am - 5:00pm: **REGISTRATION (Second Floor, Conference Lobby: 1-5)**

08:00 - 08:20am: FREE SLOT

SESSION B: **FEATURED SESSION**
DEVELOPING HETEROGENEOUS COMPUTING SYSTEMS (MULTICORE, CPU PLUS FPGA, …)
Chair: Dr Pascal Benoit, Electrical Engineering department of University of Montpellier, France
July 17, 2012 (Tuesday): 08:00pm – 10:20pm
(LOCATION: Gold Room)

08:20 - 08:40am: Identifying Data-Dependent System Scenarios in a Dynamic Embedded System
Elena Hammari*, Francky Catthoor**, Per Gunnar Kjeldsberg*, Jos Huisken***, Konstantinos Tsakalis****, Leonidas Iasemidis****
* Norwegian University of Science and Technology, Norway
** Imec and K.U.Leuven, Belgium
*** Imec / Holst Centre, The Netherlands
**** Arizona State University, USA

08:40 - 09:00am: Industrial Paper
From Streaming Models to FPGA Implementations
Hugo Andrade, Jeff Correll, Amal Ekbal, Arkadeb Ghosal, Douglas Kim,
Jacob Kornerup, Rhishikesh Limaye, Ankita Prasad, Kaushik Ravindran,
Trung N Tran, Mike Trimborn, Gerald Wang, Ian Wong, Guang Yang
National Instruments Corporation, USA

09:00 - 09:40am: Distinguished Paper
A Configurable VHDL Template for Parallelization of 3D Stencil Codes on FPGAs
Franz Richter, Michael Schmidt and Dietmar Fey, FAU Erlangen-Nuremberg, Germany

09:40 - 10:20am: Invited Talk (Moderator: Prof. Franz Richter)
Distributed Approaches for Self-Adaptive Embedded Systems
Dr Pascal Benoit, Electrical Engineering department of University of Montpellier, France

10:20 - 10:40am: BREAK

SESSION C: FEATURED SESSION
HARDWARE SECURITY AND TRUST IN RECONFIGURABLE HETEROGENEOUS SYSTEMS
Chair: Prof. Tim Güneysu, Horst Goertz Institute for IT-Security, Ruhr-Universitaet Bochum, Germany
July 17, 2012 (Tuesday): 10:40pm – 04:00pm
(LOCATION: Gold Room)

10:40 - 11:20am: Invited Talk
Tackling the Security Issues of FPGA Partial Reconfiguration with Physical Unclonable Function
Dr. Yohei Hori, **National Institute of Advanced Science and Technology, Japan**

11:20 - 12:20am: ERSA Industrial Keynote
Ensuring Design Integrity through Analysis of FPGA Bitstreams and IP Cores
Jonathan P. Graf, Scott H. Harper, and Lee W. Lerner
Luna Innovations Inc., USA

12:20 - 12:40pm: LUNCH (On Your Own)
12:40 - 01:00pm: LUNCH (On Your Own)
01:00 - 01:20pm: LUNCH (On Your Own)
01:20 - 01:40pm: LUNCH (On Your Own)

01:40 - 03:00pm: **PANEL DISCUSSION & SHORT STATEMENTS**
HARDWARE SECURITY AND TRUST IN RECONFIGURABLE HETEROGENEOUS SYSTEMS
Chair: Jonathan P. Graf, Director, Secure Computing and Communications Technologies at Luna Innovations, Luna Innovations Inc., Virginia, USA

03:00 - 03:20pm: **BREAK**

03:20 - 03:40pm: **Distinguished Paper (Moderator: Jonathan P. Graf)**
Cryptanalysis on Reconfigurable Computers
Tim Güneysu, Horst Goertz Institute for IT-Security, Ruhr-Universitaet Bochum, Germany

03:40 - 04:00pm: A Practical FPGA Implementation of Regular Expression Matching with Look-ahead Assertion
Yoichi Wakaba, Masato Inagi, Shin'ichi Wakabayashi
Hiroshima City University, Japan

SESSION D: **REGULAR SESSION**
RECONFIGURABLE ARCHITECTURE
Chair: Dr. G. Botella, Complutense University of Madrid, Madrid, Spain
July 17, 2012 (Tuesday): 04:00pm – 06:00pm
(LOCATION: Gold Room)

04:00 - 04:40pm: **Distinguished Paper**
Area-Efficeint Design of Asynchronous Circuits Based on Balsa Framework for Synchronous FPGAs
Yoshiya KOMATSU, Masanori HARIYAMA and Michitaka KAMEYAMA
Tohoku University, Japan

04:40 - 05:20pm: **Distinguished Paper**
FPGA-based Implementation of Compact Compressor and Decompressor of Floating-Point Data-Stream for Bandwidth Reduction
Tomohiro Ueno, Yoshiaki Kono, Kentaro Sano, Satoru Yamamoto
Tohoku University, Japan

05:20 - 05:40pm: Optical configuration acceleration on a new optically reconfigurable gate array VLSI using a negative logic implementation
Retsu Moriwaki and Minoru Watanabe
Shizuoka University, Japan

05:40 - 06:00pm: Architecture of an Asynchronous FPGA for Handshake-Component-Based Design
Yoshiya KOMATSU, Masanori HARIYAMA and Michitaka KAMEYAMA
Tohoku University, Japan

06:00 - 07:00pm: DISCUSSION SESSION: SHORT PAPERS & POSTERS

- **O** An Asynchronous FPGA Based on Dual/Single Rail Hybrid Architecture
  Zhengfan XIA, Shota ISHIHARA, Masanor HARIYAMA, and Michitaka KAMEYAMA
  Tohoku University, Japan

- O Watermarking-Based Protection of Embedded Cores on FPL Devices
  L. Parrilla*, E. Castillo*, A. García*, G. Botella**
  * Dept. Electronics and Computer Technology, University of Granada, Granada, Spain
  ** Dept. of Computer Architecture and Automation, Complutense University of Madrid, Madrid, Spain

- O Optimal Earliest Deadline First Preemptively Scheduling For Real-Time Reconfigurable Sporadic Tasks
  Hamza Gharsellaoui1, Mohamed Khalgui1,2,3, Samir Ben Ahmed4
  1 INSAT Institute - University of Carthago, Tunisia
  2 ITIA Institute - CNR Research Council, Italy
  3 Systems Control, Xidjian University, China
  4 FST Faculty - University of Tunis El Manar, Tunisia

- O Low-Power Heterogeneous Platform for High Performance Computing and Its Application to 2D-FDTD Computation
  Hasitha Muthumala Waidyasooriya, Yasuhiro Takei, Michitaka Kameyama
  Tohoku University, Japan

06:00 - 09:00pm: TUTORIALS + INVITED PRESENTATIONS
(Please see the lists at the beginning of the WORLDCOMP'12 Conference Schedules)